# Multi Level PWM Switched Voltage Source Inverter

**R.Kavin[1] and M.Ranjith kumar[2]**

[1]Assistant Professor Dept of EEE ECET: kavin882@gmail.com
[2] Assistant Professor Dept of EEE SVCE: ran13jith@yahoo.com

*Abstract*-**A Multilevel switched voltage source inverter is designed. It consists of three single-phase inverter modules and each module is composed of a switched voltage source and inverter switches. The major advantage is that the peak value of the phase output voltage is twice as high as that of the conventional neutral-point-clamped PWM inverter. Thus, the proposed inverter is suitable for applications with low voltage sources such as batteries, fuel cells, or solar cells. Furthermore, three-level output waveforms of the inverter can be achieved without the switch voltage unbalance problem. Since the average neutral point potential of the inverter is zero, a common ground between the input stage and the output stage is possible. Therefore, it can be applied to a transformer less power conditioning system. The SVS inverter is verified by a PSIM simulation**.

*Index Terms*- Neutral-point-clamped (NPC), Switched Voltage Source Inverter, Pulse width modulation (PWM),

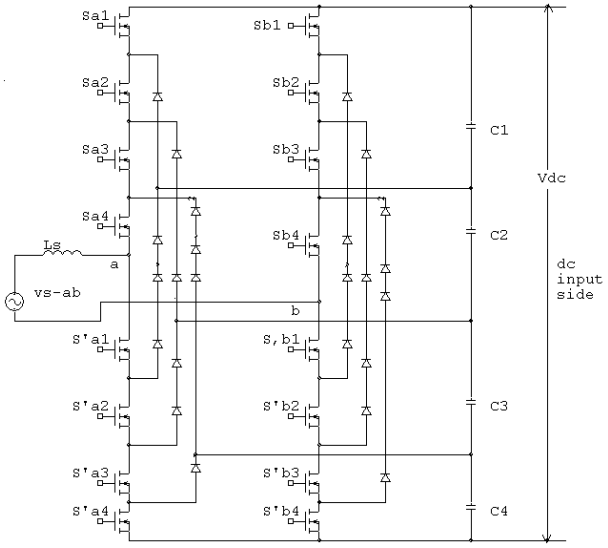
## I. INTRODUCTION

In recent years, industry has begun to demand higher power equipment. Multilevel inverters have been attracting increasing attention for power conversion in high-power applications due to their lower harmonics, higher efficiency, and lower voltage stress compared to two-level inverters. Numerous topologies for multilevel inverters have been introduced and widely studied. The most important topologies of these topologies, as shown in Fig. 1, are the diode-clamped inverter, the capacitor-clamped (flying capacitor) inverter, and the cascaded H-bridge inverter with separated dc sources. In the diode-clamped inverter as shown in Fig. 1(a), the dc-bus voltage is split into Multilevel by two series-connected bulk capacitors, and two diodes clamp the switch voltage to half of the level of the dc-bus voltage. The output voltage has three states: $V_{dc}/2$, 0, and $-V_{dc}/2$. It is noted that
Although the output voltage $V_{UN}$ is alternating current (ac), $V_{UG}$ has a direct current (dc) component. Therefore, the difference between $V_{UN}$ and $V_{UG}$ is the voltage across $C_2$, which is $V_{dc}/2$. Two series-connected switches of the diode-clamped inverter can achieve the multilevel output waveforms and reduce the voltage stress to half of the input voltage. However, the diode-clamped inverter has the unbalance of the blocking voltage between the inner and the outer devices due to the difference of the switching characteristics.

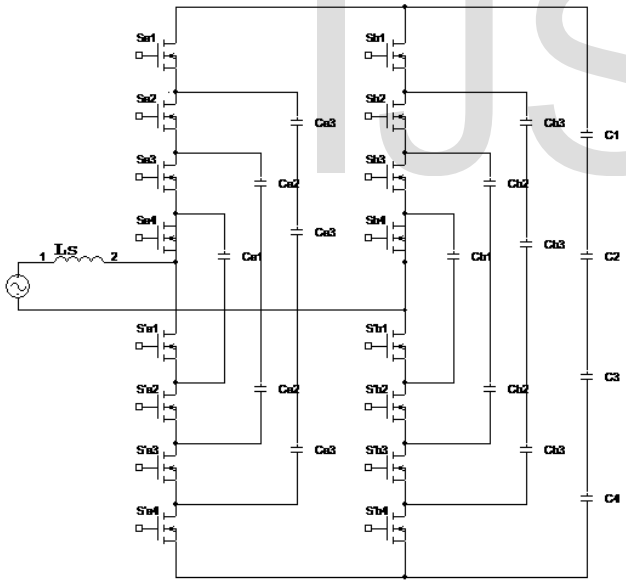
This problem results in the larger voltage stress in the inner devices Furthermore, the diode-clamped inverter has undesirable features such as a ripple in the neutral-point voltage due to the current flowing out of or into the neutral point of the dc link and steady-state unbalance in the neutral-point voltage due to a variety of factors including component imperfections, proposed a multilevel structure where the device off state voltage clamping was achieved by using clamping capacitors rather than clamping diodes as shown Fig. 1(b). Although this topology solves the problem of static and dynamic sharing of the voltage across the switches, it still has the voltage unbalance problem in the neutral-point voltage and dc offset voltage of the output.

To solve neutral-point balancing problem, various strategies have been presented. Although balancing techniques can be used to reduce the voltage unbalance in the neutral-point there are still limitations on the maximum amount of reduction. In case of the dc offset voltage of the output, if the input voltage $V_{dc}$ can be split into a positive $V_{dc}/2$ and a negative $-V_{dc}/2$ part with the midpoint connected to the neutral, the dc offset problem of the output disappears. These problems appear to be inherent to the topology. The cascaded H-bridge inverter shown in Fig. 1(c) is an alternative approach to achieve multilevel waveforms based on the series connection of full-bridge inverters with a multiple isolated dc bus. Although the modular structure solves the voltage unbalance problem, this approach requires many isolated dc sources and a link voltage controller. To solve all these drawbacks of conventional

multilevel inverters, a new three-level pulse width modulation (PWM) switched voltage source (SVS) inverter is proposed. Fig. 2 shows the circuit configuration of the proposed muti-level PWM SVS inverter. It consists of three single -SVS inverter. It consists of three single- inverter modules.



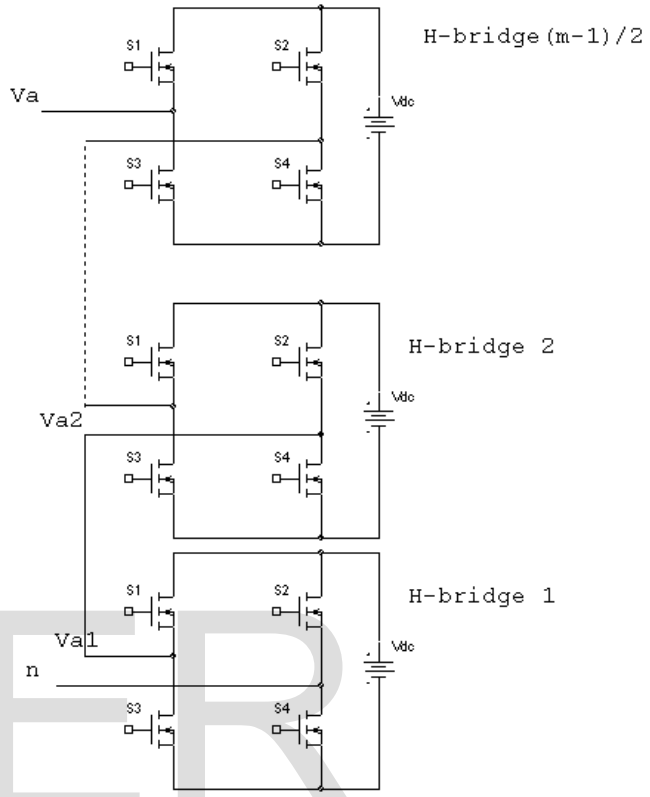

(a)




(b)

Fig.1. Major topologies of multilevel inverter: (a) diode-clamped inverter, (b) capacitor-clamped inverter, and (c) cascaded H-bridge inverter

Each module is composed of a main inverter stage and a switched voltage source stage which includes two switches, one flying capacitor, one diode and a small snubber inductor as shown in Fig. 3. It provides a three-level output across U and N, i.e.,$V_{UN=}$ $V_{dc}$ , 0, or -$V_{dc}$. Therefore, the peak value of the phase voltage is $V_{dc}$, and the peak value of the line to line voltage is $2V_{dc}$ . Since the phase voltage of the SVS inverter is twice as high as that of the conventional NPC inverter,




(c)

it is well suited for inverters with a low input voltage such as a fuel cell, battery, and solar cell. In addition, the SVS inverter does not have the voltage unbalance problem which is often the case with the conventional three-level inverters with a divided input source. Furthermore, since the dc offset of the output phase voltage is zero,

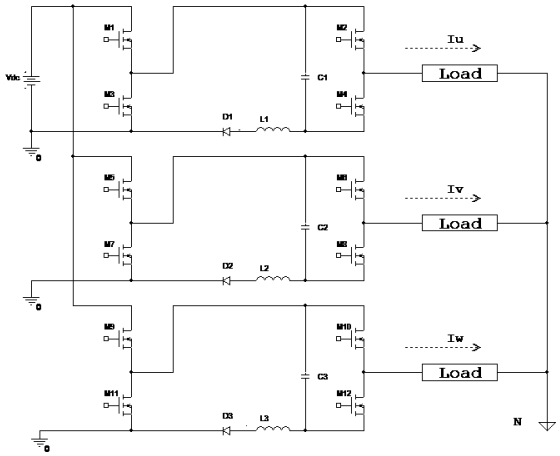



Fig. 2. Circuit diagram of the proposed SVS inverter.

The neutral point of the output load stage can be connected to the ground, and the SVS inverter is safe without an electrical isolation. Therefore, it can easily be applied to a transformerless power conditioning system.

## II. OPERATIONAL PRINCIPLES

### A. Circuit Operation

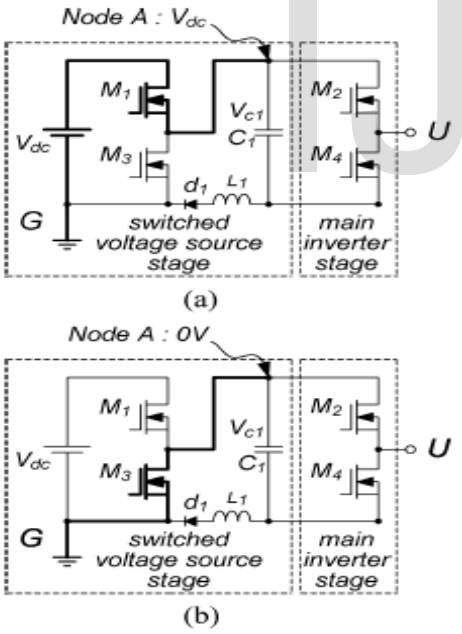



Fig. 3.Operational principles of switched voltage source: (a)Node A: $V_{dc}$ and (b) node A: 0 V.

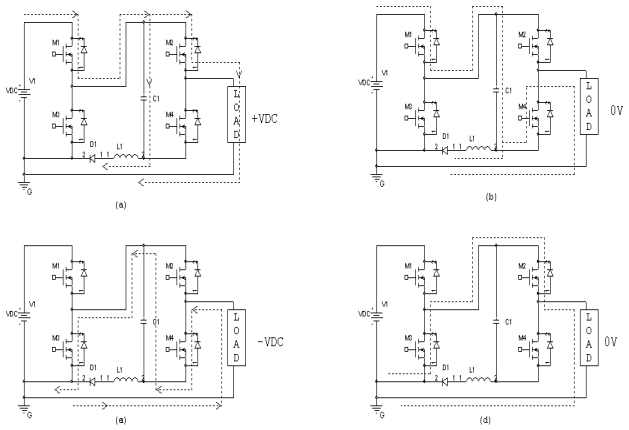



Fig. 4. Operational modes of three-level inverter: (a) $V_{UG} = V_{dc}$ (b) $V_{UG} = 0V$, (c) $V_{UG} = -V_{dc}$ ,and (d)$V_{UG} = 0V$.

The circuit configuration of the three-level PWM SVS inverter consists of three single-phase inverter modules as shown in Fig. 2. Each module can be independently operated with a single input source. The basic operational modes of the SVS inverter are shown in Figs. 3 and 4. Since the flying capacitor $C_1$ is charged to input voltage $V_{dc}$ when the switch $M_1$ turns on, voltage across $C_1$ can be assumed to be a constant voltage source $V_{dc}$ and snubber inductor $L_1$ can be ignored. As can be seen in Fig. 3, the voltage of node A can be changed to input voltage $V_{dc}$ and 0 V by switch $M_1$ and $M_3$, respectively. The difference between node A and U is 0 and $-V_{dc}$ by switch $M_2$ and $M_4$, respectively, as shown in Fig. 4. Therefore, the SVS inverter has four different cases and three states of the output terminal voltage $V_{UG}$: $V_{dc}$ , 0, and $-V_{dc}$ which are twice those of the conventional NPC inverter. Furthermore, does not have a dc component.

Case 1) [Fig. 4(a)]: The output voltage $V_{UN}$ is $V_{dc}$ and $C_1$ is charged to $V_{dc}$ , when switches $M_1$ and $M_2$ turn on. The snubber inductor limits the inrush current $M_1$ of when the voltage of $C_1$ is different from $V_{dc}$.

Case 2) [Fig. 4(b)]: The output voltage $V_{UN}$ is 0 V when switches $M_1$ and $M_4$ turn on.

Case 3) [Fig. 4(c)]: When switches $M_3$ and $M_4$ turn on, the diode $D_1$ turns off. In addition, the output voltage $V_{UN}$ is clamped to $-V_{dc}$ and the flying capacitor $C_1$ is discharged.

Case 4) [Fig. 4(d)]: The output voltage is 0 and diode $D_1$ is off, when switches $M_3$ and $M_4$ turn on.

The same analysis can also be applied to the other modules

## III. ANALYSIS OF THE PROPOSED INVERTER

In the preceding section, the voltage across capacitor $C_1$ of the switched voltage source (SVS) stage shown in Fig. 2 was assumed to be a constant voltage source Vdc. However, the voltage across the capacitor $C_1$, $V_{C1}$ is slightly different from the input voltage source $V_{dc}$ The difference between the voltage across the capacitor $C_1$ and the input voltage source $V_{dc}$ may cause an inrush current on the switch $M_1$ and diode $D_1$ when the switch $M_1$ turns on... To solve this problem, a small snubber inductor $L_1$ is inserted between the diode $D_1$ and capacitor $C_1$. However, this small snubber inductor does not affect the operation of the proposed SVS inverter. The effect of the small snubber inductor $L_1$ is considered in this section Fig. 5 shows the circuit operation when $V_{REF,1} < V_{TRI,2}$ , and Fig. 6 show buckcircuit. The SVS stage shown in Fig. 2 is operated as a buck converter as seen in Figs.5 and 6.

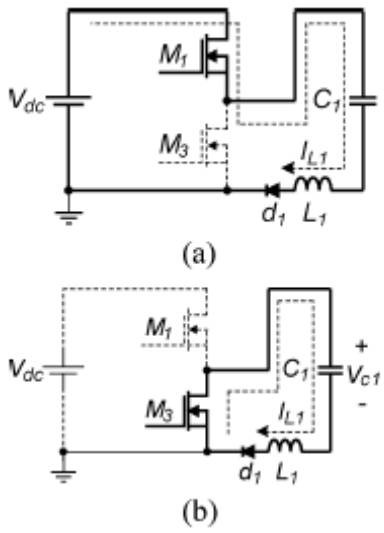



Fig. 5. Operation of the SVS inverter: (a) powering mode and (b) freewheeling mode.

Therefore, to analyze the operation of the SVS stage according to the value of the inductor, the simple buck converter can be considered.

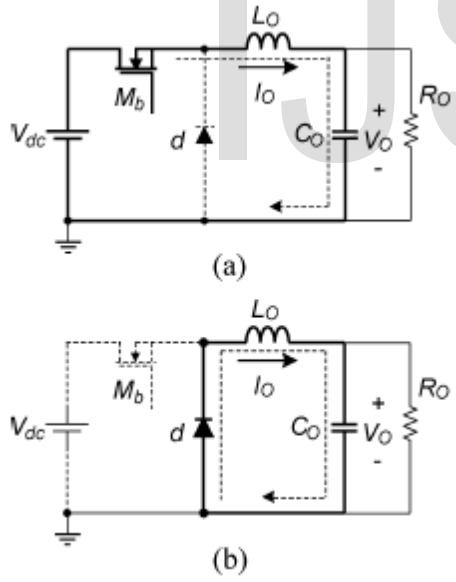



Fig. 6. Buck converter: (a) powering mode and (b) freewheeling mode

If the snubber inductor $L_1$ is small, the buck converter operates in discontinuous conduction mode (DCM). When the buck converter is operated in DCM, its voltage conversion ratio is expressed as

$$M = \frac{V_O}{V_{dc}} = \frac{2}{1+\sqrt{1+\frac{8TL}{D^2}}}$$

Where

$T_L$ $(L_O/R_O.T_S) = L_O.I_O/(V_O.R_S)$

$T_S$ switching period;

D duty ratio;

$L_O$ filter inductance;

$R_O$ load resistance.

Based on this equation, the voltage conversion ratio can be plotted as shown in Fig. 8. This figure shows that the less inductance can make the voltage conversion ratio M close to the unity for a wide range of the duty ratio. In the case of the laboratory prototype, the modulation index $m_a$ is less than 0.8, and the duty ratio of the switch $M_1$ is greater than 0.2. Also, the parameter $T_L$ is about 0.0005, and the voltage conversion ratio M at D=0.2 is 0.976. This means that the difference between the voltage across the capacitor $C_1$ and the input voltage source $V_{dc}$ is 2.4%.

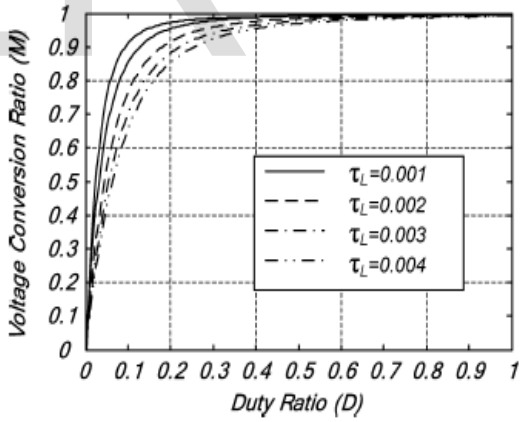



Fig. 7. Voltage conversion ratio in the DCM buck converter.

Therefore, $V_{c1}$ can be assumed to be a voltage source charged with $V_{dc}$ . In addition, the design equation of $L_1$ can be derived from (2) and expressed as

$$L_1 = R_O.T_S.\frac{D^2}{8}.\left\{\left(\frac{2}{M}-1\right)^2-1\right\} \quad (3)$$

$$=\frac{V_{C1}}{I_{L1}}.T_S.\frac{(1-m_a)}{8}.\left\{\left(\frac{2}{M}-1\right)^2-1\right\} \quad (4)$$

Where

$T_S$ switching period;

D duty ratio;

$R_O$ load resistance;

$m_a$ modulation index.

If the rated output voltage, the rated output current, and the allowed error of the output voltage are known, the proper value of inductance $L_1$ and modulation index $m_a$ can be determined from (4).

## IV. EXPERIMENTAL RESULTS

The operational principles of the SVS inverter shown in Fig. 2 have been investigated by PSIM simulation. Fig.8.show the simulated results of the phase voltages, line to line voltages, and load currents of the multi-level voltage source inverter, respectively. As can be seen in Fig.8, the peak value of the phase voltages is 200 V and the peak value of the line to line voltage 2 is 400 V. These are twice as high as those of the conventional NPC inverter. Therefore, the larger amplitude of the output voltage can be obtained compared with the conventional NPC inverter and it is well suited for an inverter with a low input voltage source

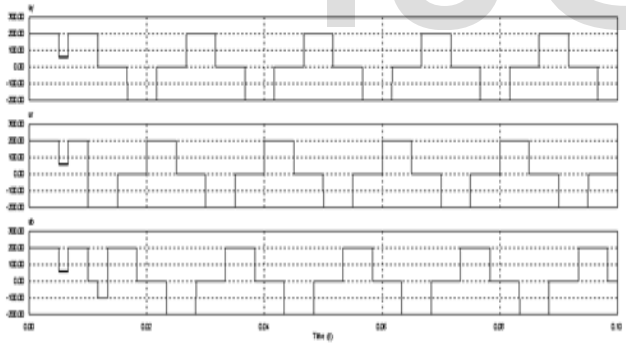


Fig 8.Output phase voltage of svs inverter

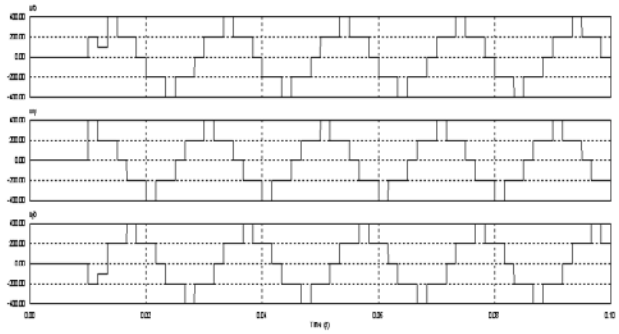


Fig 9. Output line voltage of svs inverter

## VI. CONCLUSION

A new multilevel SVS inverter with zero neutral point potential is proposed. Its phase voltage and line to line voltage are twice as high as those of the multi-level waveform can be achieved without the switch voltage unbalance problem. Therefore, it is well suited for an inverter with low input voltage such as a fuel cell, battery, or solar cell input. Furthermore, its average neutral point potential is zero. Therefore, the proposed SVS inverter can be widely applied to motor drive systems and transformerless grid connected power conditioning systems.

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